AMENDMENTS TO THE CLAIMS:

Please cancel claims 1, 2, and 19, without prejudice or disclaimer and amend claims 3 and 20, as listed in the following listing of the claims, which replaces all prior versions and listings of claims in the application:

1. (Canceled).

2. (Canceled).

3. (Currently Amended) An ~~The~~ apparatus for processing data, comprising: ~~according to claim 2, further comprising~~

a plurality of input signal lines;

a plurality of output signal lines;

an electronic circuit configured to input first data from the plurality of input signal lines and to output second data to the plurality of output signal lines, the first data being one bit data represented by a combination of bits of the plurality of input signal lines, and the second data being one bit data represented by a combination of bits of the plurality of output signal lines,

wherein the combination of bits of the plurality of signal lines of the one bit data "0" is a first bit status, the combination of bits of the plurality of signal lines of the one bit

data "1" is a second bit status, and a hamming weight of the first bit status is equal to a hamming weight of the second bit status; and

an input unit configured to input a control signal representing a distinction between a working phase and an idle phase, the working phase being a period to input and output the first bit status or the second bit status, and the idle phase being a period to input and output a third bit status as the combination of bit status of the plurality of signal lines of invalid data.

4. (Original) The apparatus according to claim 3,

wherein the idle phase is inserted between two working phases neighbored on a time axis.

5. (Original) The apparatus according to claim 3,

wherein the hamming distance between the first bit status and the third bit status is equal to the hamming distance between the second bit status and the third bit status.

6. (Original) The apparatus according to claim 5,

wherein the plurality of input signal lines and the plurality of output signal lines are respectively two as a first signal line and a second signal line.

7. (Original) The apparatus according to claim 6,

wherein the first bit status is a combination of the bit "1" of the first signal line and the bit "0" of the second signal line or a combination of the bit "0" of the first signal line and the bit "1" of the second signal line,

wherein the second bit status is an inverse of the first bit status, and

wherein the third bit status is a combination of the bit "0" of the first signal line and the bit "0" of the second signal line or a combination of the bit "1" of the first signal line and the bit "1" of the second signal line.

8. (Original) The apparatus according to claim 3,

wherein said input unit inputs a clock signal of which period between a rise edge and a fall edge is shorter than a period of the working phase of the control signal, and of which period between a rise edge and next rise edge is larger than the period of the working phase of the control signal.

9. (Original) The apparatus according to claim 8,

wherein, if the control signal represents the working phase, said electronic circuit inputs the one bit data of the first bit status or the second bit status from the plurality of input signal lines based on the clock signal, and holds the one bit data.

10. (Original) The apparatus according to claim 9,

wherein, if the control signal represents the next working phase, said electronic circuit outputs the one bit data held to the plurality of output signal lines based on the clock signal.

11. (Original) The apparatus according to claim 10,

wherein, if the control signal represents the idle phase, said electronic circuit does not input the invalid data from the plurality of input signal lines.

12. (Original) The apparatus according to claim 11,

wherein, if the control signal represents the idle phase, said electronic circuit outputs predetermined invalid data to the plurality of output signal lines based on the clock signal.

13. (Original) The apparatus according to claim 9,

wherein said input unit inputs the one bit data at a rate of one time in two times of the rise edge or the fall edge of the clock signal.

14. (Original) A logical operation apparatus, comprising:

a first data holding circuit configured to input one bit data represented by a combination of bits of two signal lines, to temporarily store the one bit data, and to output the one bit data;

a second data holding circuit configured to input one bit data represented by a combination of bits of other two signal lines, to temporarily store the one bit data, and to output the one bit data;

a first logical operation circuit configured to execute a logical operation of a first input data and a second input data, the first input data being a bit status of a first output signal line of the first data holding circuit, the second input data being a bit status of a first output signal line of the second data holding circuit;

a second logical operation circuit configured to execute a logical operation of a first input data and a second input data, the first input data being a bit status of a second output signal line of the first data holding circuit, the second input data being a bit status of a second output signal line of the second data holding circuit; and

a third data holding circuit configured to input one bit data represented by a combination of bits of an output signal line of the first logical operation circuit and an output signal line of the second logical operation circuit.

15. (Original) The logical operation circuit according to claim 14,

wherein the first logical operation circuit executes AND operation of the first input data and the second input data, and

wherein the second logical operation circuit executes OR operation of the first input data and the second input data.

16. (Original) The logical operation circuit according to claim 14,

wherein the first logical operation circuit executes OR operation of the first input data and the second input data, and

wherein the second logical operation circuit executes AND operation of the first input data and the second input data.

17. (Original) The logical operation circuit according to claim 14,

wherein the first logical operation circuit executes NAND operation of the first input data and the second input data, and

wherein the second logical operation circuit executes NOR operation of the first input data and the second input data.

18. (Original) The logical operation circuit according to claim 14,

wherein the first logical operation circuit executes NOR operation of the first input data and the second input data, and

wherein the second logical operation circuit executes NAND operation of the first input data and the second input data.

19. (Canceled).

20. (Currently Amended) A ~~The~~ logical operation apparatus, comprising:~~according to claim 19, further comprising:~~

a first data holding circuit configured to input one bit data represented by a combination of bits of two signal lines, to temporarily store the one bit data, and to output the one bit data by a first output signal line and a second output signal line;

a second data holding circuit configured to input one bit data from a first input signal line and a second input signal line, the one bit data being represented by a reverse combination of bits of the first output signal line and the second output signal line, to temporarily store the one bit data, and to output the one bit data;

a first inverter configured to input a bit status of the first output signal line, and to output a reverse status of the bit status to the first input signal line of the second data holding circuit; and

a second inverter configured to input a bit status of the second output signal line, and to output a reverse status of the bit status to the second input signal line of the second data holding circuit.